TAU-800B *Super*

Quick-start guide

TEST PROGRAM 1 — DOT PRODUCT

(NO TIME ADDRESSING)

ADD CH BH (ADD UPPER BITS, NO NEED TO JSR CARRY) (2)

SEC (CLEAR BORROW FLAG)

SUB #01 X (SETS NVZ)

BEQ +3

JMP (?) → 3b02 (~~NEED TO CALCULATE~~)

MOVE TO DISPLAY:

MOV BL %0087

MOV BH %0187

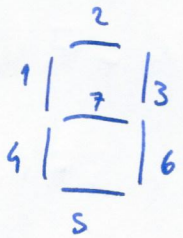
NOP

CLC

BCC -4 → CARRY

ADD #01 BH

RET



1 — 1, 4
2 — 2, 3, 7, 4, 5
3 — 2, 3, 5, 6, 7
4 — 1, 7, 3, 6
5 — 1, 2, 7, 5, 6
6 — 1, 2, 4, 3, 6, 7

7 — 2, 3, 6
8 — 1, 2, ..., 7
9 — 1, 2, 3, 6, 7

SOC-B Quick

Start Guide

This is a quick-start guide to your Time Arithmetic Unit (Revision 800B, *Super* edition) time-assisted computing machine. Please ensure you have thoroughly read and understood the User Manual and the Warranty Disclaimer before attempting to utilize the machine. Jikan Systems Corp.© is not responsible for any damages resulting from improper use of the time jump facilities of this machine.

Please ensure that the Novikov module has sufficient power throughout the operation of the machine. Failure to supply the minimum rated power may cause time inconsistency paradoxes.

In the unlikely case of forced inconsistency contact our hotline

1-800-NOTIME

Contents

1 Introduction

Congratulations on becoming the proud owner of a Time Arithmetic Unit (Revision 800B, *Super* edition), the latest technology in time-based computing. The following document serves as an introduction to the architecture and operation modes of this time-assisted arithmetic computing unit as well as to any other extensions offered by Jikan Systems Corp.© compatible with the TAU-800B *Super* that were acquired as part of your commercial agreement.

For more information regarding available computing extension hardware compatible with your computing unit contact your local Jikan Systems Corp.© sales representative. Missing documentation of acquired computing extension hardware and advanced time operation modes of the computing unit can be obtained upon written request with proof of purchase to Jikan Systems Corp.© Hanshin Main Headquarters.

Please note that this document does not preclude the consultation of the complete reference manual, which should have been provided to you alongside this document and the computing unit. If the complete reference manual was not provided to you upon purchase, please contact your local sales representative.

Jikan Systems Corp.© is not liable for damages incurred in the misuse of the equipment to the extent of but not limited to the operation modes described in this document.

2 Self-consistent Novikov-Turing Assisted Computing

The TAU-800B *Super* provides new computing advances by exploiting the well-known Novikov-Turing speedup, schematized in figure 1 for convenience. These modes of operation are seamlessly exposed via the assembly language (see section 3). Please refer to the complete reference manual for examples of implementation of some of the known temporal computing speedups.

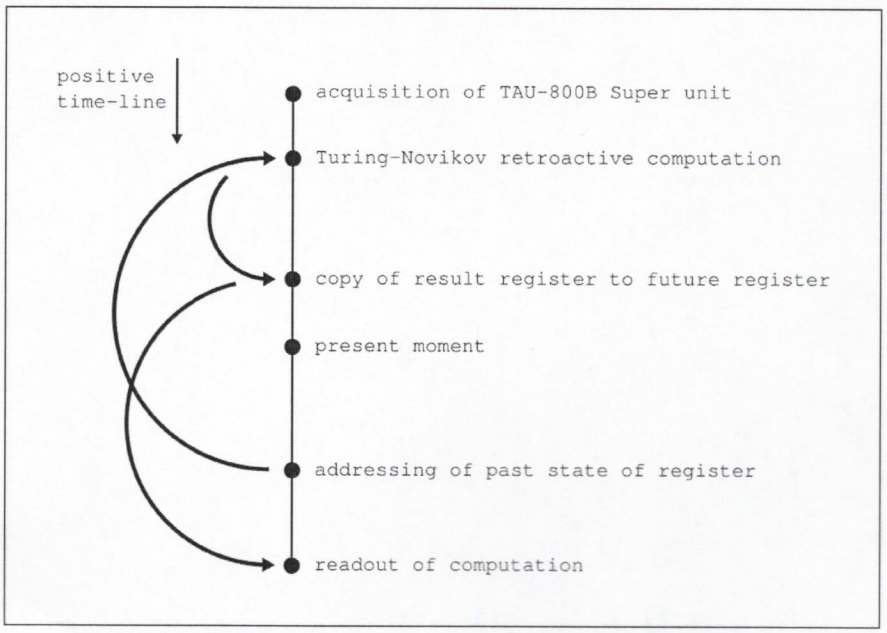


Figure 1: The Turing-Novikov effect at play in the TAU-800B *Super* modes of operation. The Novikov stability module (full reference manual, sec. 4, fig. 10, schematic 1 a)), ensures self-consistency in the computing process.

The TAU-800B *Super* architecture was designed to reproduce as closely as possible (within technical limits) the theoretical model typically employed for causal-consistency calculations, so as to facilitate the transposition from theoretical programs with consistency speedups into operation. In figure 2, a schematic of a high-level overview of the architecture is presented, where each component in the schematic broadly encompasses various physical elements of the machine. For a complete description of these physical elements, please refer to the Service and Schematics section of the complete reference manual.

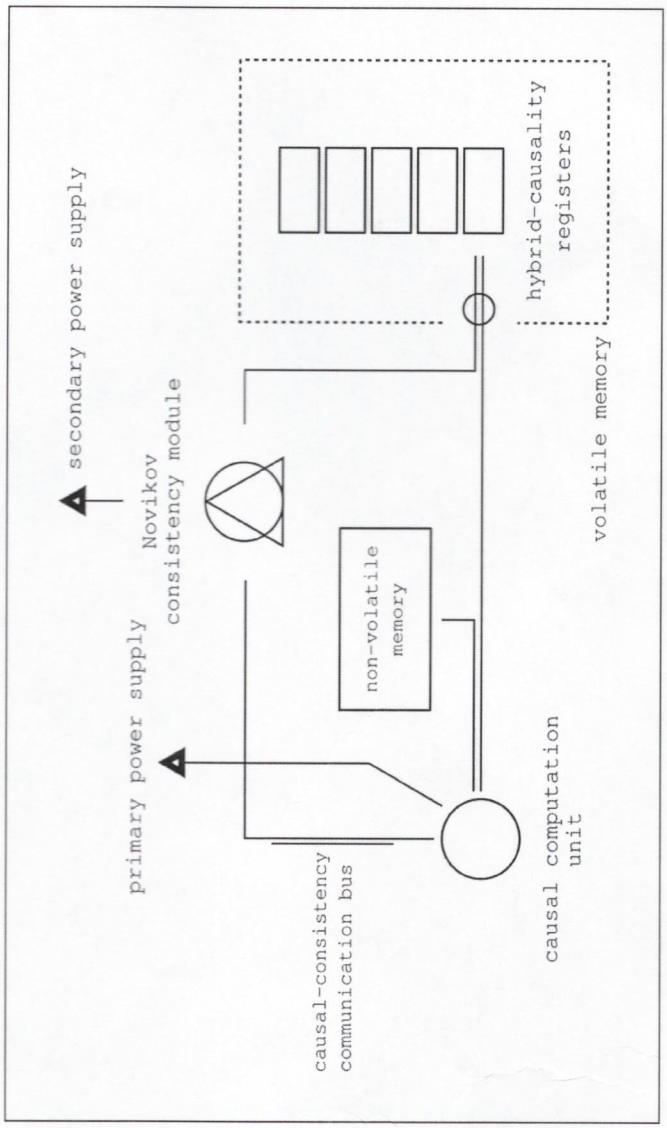


Figure 2: High-level overview of causal-consistent hardware architecture.

3 The Machine Language

The following is a quick-reference guide to TAU-800B *Super* assembly language. Please use ONLY the officially licensed assembler programs by Jikan Systems Corp.©. [1]

Quick facts:

- 6-bit word size, 12-bit address space with pageable memory.
- 0.66 MHz clock speed.
- Four general purpose word registers.
- Six-word stack.
- Time jumps of up to 200 clock cycles in any direction.[2]
- Memory-mapped IO.
- Big endian.

CPU registers

The CPU has a total of 10 (ten) words of register memory. Of these, 5 (five) words are general-purpose registers and 5 (five) are special-purpose registers.

The general purpose registers are the following: `A`, `BH`, `BL`, `CH`, `CL`. The latter two pairs of registers can be used to store 2-word values, high word and low word respectively. These registers are used readable and writable via move and arithmetic-logic instructions.

Then, the CPU has one flag register `F`, with the following bits: `NV--ZC`, respectively negative, overflow, zero, and carry flags. These are set and cleared by arithmetic and logical instructions, and can be queried by the conditional branch instructions. The flag register cannot be written to, but it can be read and copied to memory or another register.

The `X` register is an index register: it can be read and written to like a general purpose register, and it can be used in the indexed addressing mode to access a location obtained by adding the contents of the register to a base address.

The CPU also has a stack pointer, that points to one-past the top of the stack. It can be read or written to as a general purpose register, but it is also altered by the `CAL`, `RET`, `PSH`, `POP` instructions.

Finally, the two-word program counter stores the address of the next instruction, and can be modified by jump, branching and subroutine instructions

12-bit addresses are read and stored as two words in big-endian order: `%llhh`. In order to perform 12-bit arithmetic, you must process the two words manually.[3]

Contact sales...

[1] If you have not been supplied with all 9 (nine) floppy diskettes for installation of the assembler, please contact your local sales representative.

[2] Note: for jumps of over 80 clock cycles an upgraded SPS-3-6000 power supply with at least 6 kW of peak power output must be provided. **Serious damage may occur if you attempt to use these operations without sufficient power!** Please refer to section 4 and the complete reference manual for more information.

[3] Advanced mathematical subroutines are available for purchase, please contact your regional sales representative.

Addressing modes

The following addressing modes are available:

Mode	Notation	Description
Register	`a`	a named register
Immediate	`#ff`	represents a literal one-word value
Absolute	`%llhh`	the memory address `ll` $+ 2^6 \times$ `hh`
Indexed	`%llhh,X`	the memory address `ll` $+ 2^6 \times$ `hh` + contents of `X`
Indirect	`(%llhh)`	the address stored at memory address `ll` $+ 2^6 \times$ `hh`
Indirect	`(r)`[4]	the address stored at memory address `rl` $+ 2^6 \times$ `rh`

Furthermore, the jump, call, and branch instructions require the following operands:

Mode	Notation	Description
Address	`llhh`	Absolute address
Offset	`ff`	Signed offset written as a two's complement word

Temporal addressing

Any addressing mode detailed in the first table may be suffixed with `@+dd` or `@-dd` for a temporal addressing of `dd`[5] clock cycles into the future or into the past, respectively. The assembler will automatically compute the correct surge voltage to produce the desired time jump.

> **Over-"Clocking"**
>
> **DO NOT** attempt to alter the operating clock frequency of the TAU computing unit by tampering with the clock generator in the causal-consistency bus. Damaging the warranty breakaway sticker on your TAU computing unit will immediately void your warranty. Jikan Systems Corp.© cannot be held responsible for accidents resulting from operating the TAU computing unit at non-standard clocking speeds.

List of instructions

The following is a quick-reference list of instructions.

Note: unless otherwise noted, instructions that 「set the `Z` flag」 set it if the result is zero, and clear it otherwise, instructions that 「set the `N` flag」 set it to the value of the most significant bit of the result (i.e. set if negative, clear otherwise); and instructions that 「set the `V` flag」 set if signed arithmetic overflows, and clear it otherwise..

[4] Where `r` is `b` or `c`.
[5] A decimal number.

0x0 — Registe
0x1 — Immediate
0x2 — Absolute
0x3 — Indirect
0x4 — Abs + reg

Opcodes

Memory

0x01

`MOV src dst` — Set word at `dst` to contents of `src`.
Flags: set `Z`, `N`.

`PSH src` — Push `src` onto the stack and increment `sp`.

`POP dst` — Pop value on the top of the stack onto `dst` and decrement `sp`.
Flags: set `Z`, `N`.

Arithmetic

`ADD src dst` — Set word at `dst` to `dst` + `src` + `C`.
Flags: set `Z`, `N`, `V`, set `C` on overflow.

`SUB src dst` — Set word at `dst` to `dst` − `src` − $\overline{\texttt{C}}$.
Flags: set `Z`, `N`, `V`, set `C` on underflow.

`MUL src dst` — Set word at `dst` to the lower bits of `dst` × `src`.
Flags: set `Z`, `N`.

`MUH src dst` — Set word at `dst` to the upper bits of `dst` × `src`, where operands are unsigned values.
Flags: set `Z`, `N`, Type, V makes no sense here...

`MUS src dst` — Set word at `dst` to the upper bits of `dst` × `src`, where operands are signed values.
Flags: set `Z`, `N`.

`DIV src dst` — Set word at `dst` to `dst` ÷ `src`, where operands are unsigned values.
Flags: set `Z`.

`MOD src dst` — Set word at `dst` to `dst` mod `src`, where operands are unsigned values.
Flags: set `Z`.

`AND src dst` — Set word at `dst` to bitwise-and of `src` and `dst`.
Flags: set `Z`, `N`.

`OR src dst` — Set word at `dst` to bitwise-or of `src` and `dst`.
Flags: set `Z`, `N`.

`XOR src dst` — Set word at `dst` to bitwise-xor of `src` and `dst`.
Flags: set `Z`, `N`.

`NOT dst` — Set word at `dst` to bitwise-not of `dst`.
Flags: set `Z`, `N`.

`LSL dst` — Shift bits in `dst` to the left.
Flags: set `Z`, `N`, set `C` on overflow.

`LSR dst` — Shift bits in `dst` to the right.
Flags: set `Z`, `N`.

Comparison

`CMP src dst`	Flags: set `C` to `src` > `dst`, set `Z` to `src` = `dst`.
`BIT src dst`	Flags: set `Z` to ¬(`src` ∧ `dst`).

Jump

`JMP addr`	Jump execution to `addr` (two-word address).

Branching

`BCC off`	Branch to `pc` + `off` if `C` clear (signed offset).
`BCS off`	Branch to `pc` + `off` if `C` set (signed offset).
`BNE off`	Branch to `pc` + `off` if `Z` clear (signed offset).
`BEQ off`	Branch to `pc` + `off` if `Z` set (signed offset).
`BPL off`	Branch to `pc` + `off` if `N` clear (signed offset).
`BMI off`	Branch to `pc` + `off` if `N` set (signed offset).

Control

`CLC`	Clear carry flag
`SEC`	Set carry flag

Subroutines

`CAL addr`	Store current `pc` in stack, increment `sp`, and jump to `addr`.
`RET`	Read `pc` from stack, decrement `sp`, and jump.

Miscellaneous

`NOP`	No-op.

Memory map

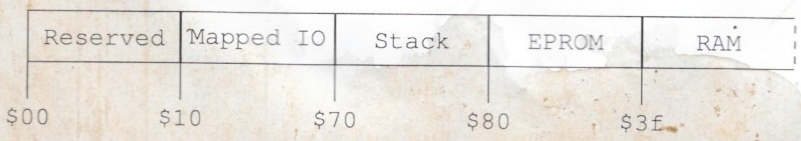
Upon power-on, the system boots from memory location `$80`. In order to write addresses `$80–$3f`, you have to reprogram the EPROM; please refer to technical procedure §8.2 in the User's Manual.

The initial stack location is `$7f`, and the stack grows downwards. It is the user's responsibility to avoid overflows and corruption of protected memory locations!

Memory locations `$10–$6f` control the unit's IO devices and peripherals. For more details, please refer to the manual of your specific device or peripheral.

Use only Approved Genuine Devices®from Jikan Systems Corp.©, its partners, and approved vendors. Jikan Systems Corp.© is not responsible for any damage sustained while an unapproved device or peripheral is connected to your unit.

The memory-map is summarised in section 3.



$10 – $14
Clock (RTC)
Module words

$15 — $16
Display Output
(See manual for map)

$45 — Module Status Interface

$16 — ...
Others (I/O)
(Depends on plug order!)

(Others are done with clock line & addressing to system — useful but unusual?)

4 Power Consumptions

Fundamental energetic lower bounds are imposed by the Novikov-Carnot-Landauer principle. Therefore, despite the high efficiency and stability of Jikan Systems Corp.© components, the TAU-800B *Super*'s power consumption is variable with temperature and operation mode. In figure 4, we provide for convenience empirical Power Consumption/Temperature curves, obtained in standard conditions. However, *for optimal performance, we recommend that you characterize your TAU-800B Super unit, and adjust your power supply to provide power accordingly.*

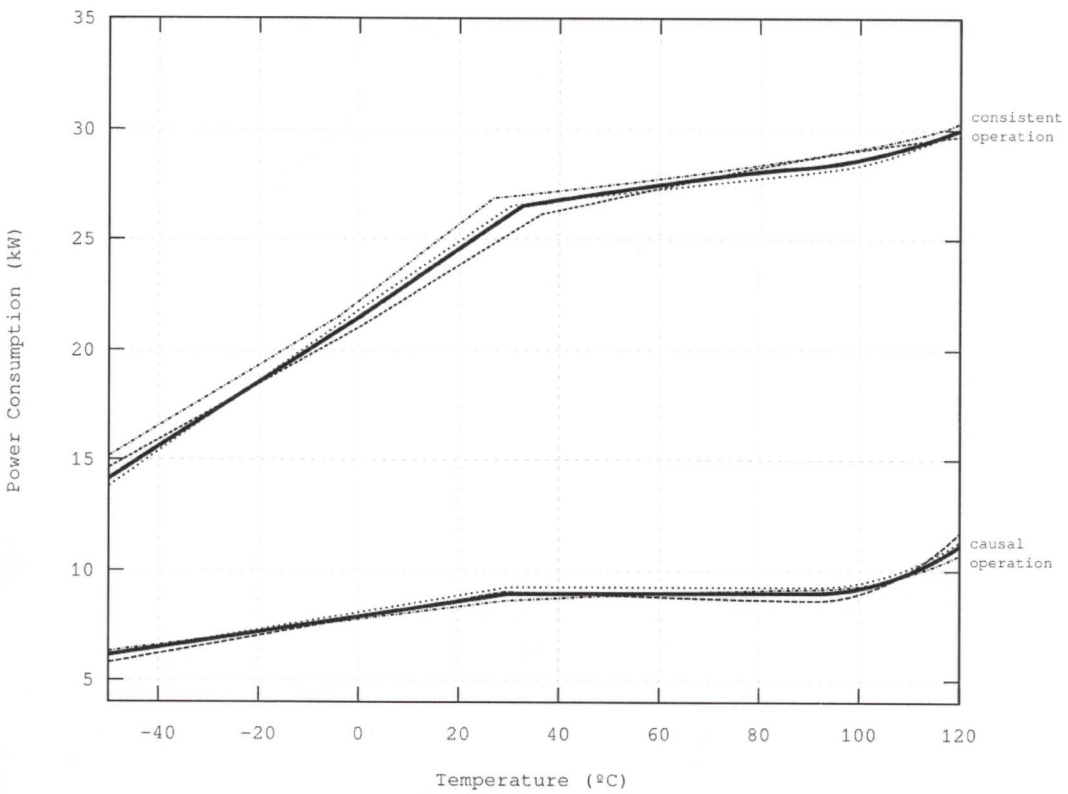


Figure 4: Experimental power consumptions for varying temperature per operating mode of the TAU-800B *Super* (Primary Power Supply). Data obtained in standard conditions and interpolated to normal distribution.

The Novikov module must be powered separately, typically with a buffer SPS-3-5000 or SPS-3-6000 module between mains and the module. **To avoid catastrophic failure, the secondary power supply *must* be able to provide constant minimum ratings throughout operation.** The SPS-3-* modules provide brown-out detection, and are therefore highly recommended. The exact required ratings can be found in the service manual provided separately with the Novikov components. If this manual was not provided to you, **do not** operate the machine and contact your sales representative. *Typical* ratings are provided, for convenience, in figure 5.

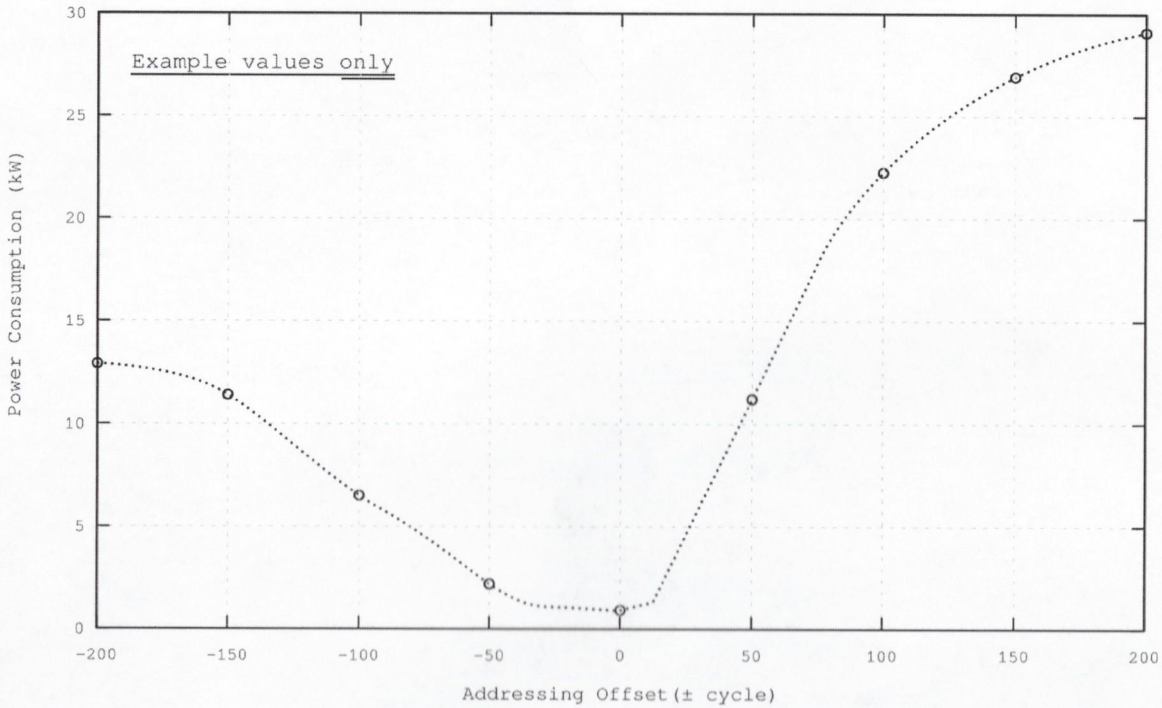


Figure 5: *Typical* power ratings (Secondary Power Supply) for varying temporal offsets in the Novikov module. **These values are for comparison *only***. You must characterize and ensure correct ratings for your Novikov module. The installation technician should have characterized and provided the ratings for your machine in the complete reference manual.

5 I/O Via the Card Tray

The I/O is done via 80-column card, inserted in the Input Tray as shown in figure 6. TAU-800B *Super* units are compatible with various formats of Program Card, and may require a different setup for compatibility. Therefore, much of this information may not be relevant for you, wherefore we refer to the complete reference manual ("Program Card Input Tray" section) for more information.

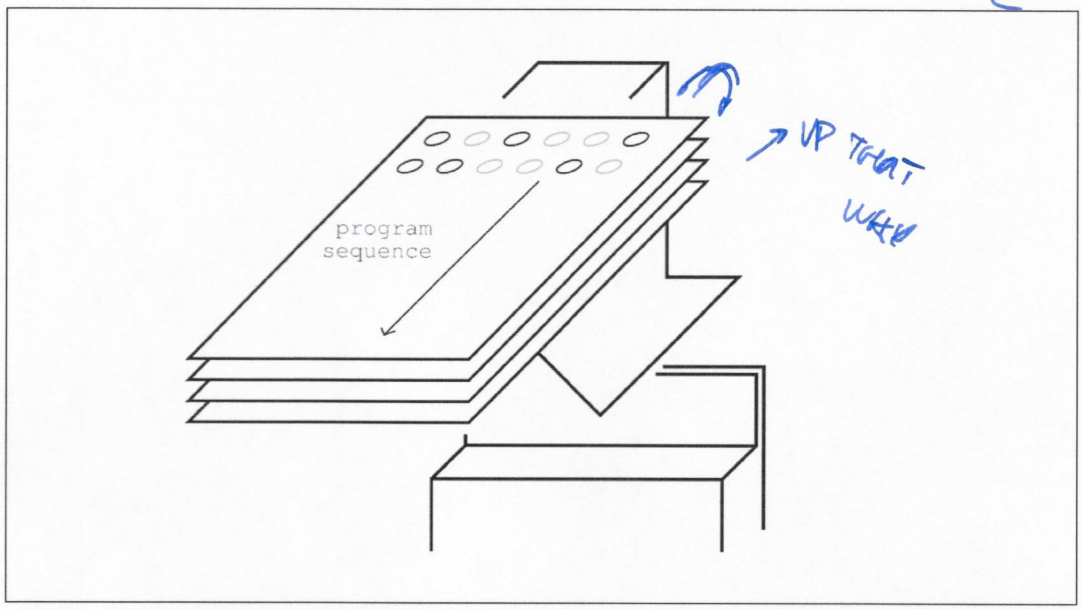


Figure 6: Program Cards are inserted in the Input Tray as shown.

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